Aggregation Switch Dynamic Buffer Management for Microburst Absorption - Official Technical Overview & Hardware Datasheet

EXECUTIVE SUMMARY

The increasing convergence of storage, compute, and latency-sensitive applications onto a single Ethernet fabric has exposed a critical flaw in traditional switch design: static buffer allocation. In modern datacenter and campus aggregation layers, traffic patterns are inherently bursty. Microbursts—short, intense periods of congestion lasting microseconds to milliseconds—can overflow shallow, fixed buffers, leading to packet drops, TCP retransmissions, and measurable application performance degradation.

The Aggregation Switch Dynamic Buffer Management (DBM) platform is purpose-built to absorb these microbursts without dropping a single packet. By combining a high-capacity, fully shared packet buffer memory pool with an intelligent, real-time arbitration engine, this platform delivers deterministic latency and zero-loss forwarding even under severe incast and many-to-one traffic conditions. This document details the hardware architecture, silicon-level capabilities, and operational logic that make this switch an ideal aggregation tier solution for hyperscale, enterprise, and carrier-grade networks.



HARDWARE ARCHITECTURE & SILICON

At the heart of the Dynamic Buffer Management platform lies a purpose-designed, high-bandwidth switching ASIC. Unlike conventional merchant silicon that partitions buffer memory rigidly per port or per port-group, this ASIC implements a fully shared, on-chip packet memory architecture. This memory pool is dynamically allocated in real time across all ingress and egress queues based on instantaneous traffic load and configured QoS policies.

The architecture employs a multi-stage, cut-through forwarding pipeline with deep packet inspection capabilities at line rate. The buffer management unit (BMU) operates independently of the forwarding pipeline, allowing simultaneous buffer allocation decisions and packet forwarding without

introducing head-of-line blocking or additional latency. The silicon supports programmable buffer thresholds, alpha-based dynamic thresholding, and per-queue byte counters for granular telemetry.

KEY FEATURES & ROUTING LOGIC

- Fully Shared Buffer Pool: A large, unified on-chip memory pool is available to all ports, eliminating the inefficiency of per-port static allocation. Under microburst conditions, idle ports release their buffer share to congested egress queues instantly.
- Dynamic Threshold Algorithm: The switch continuously monitors egress queue depth and global buffer occupancy. It dynamically adjusts the maximum allowable buffer for each queue based on the current free memory, ensuring fair sharing while maximizing burst absorption capacity for every port.
- Microburst Absorption: The platform is validated to absorb bursts of up to 100% line rate for durations exceeding 10 milliseconds on multiple ports simultaneously without packet loss, far exceeding the capabilities of standard 1RU fixed-buffer switches.
- Incast and Many-to-One Mitigation: Advanced congestion management, including Priority Flow Control (PFC) and Explicit Congestion Notification (ECN), works in concert with DBM to prevent PFC storms and eliminate deadlocks in lossless Ethernet deployments such as RoCEv2 and NVMe-oF.

- Per-Queue Telemetry: Real-time histogram and watermark statistics per egress queue provide unprecedented visibility into microburst behavior, enabling network operators to tune thresholds and validate application SLAs.

COMPLIANCE & STANDARDS

The Aggregation Switch Dynamic Buffer Management platform complies with the following industry standards and directives:

- IEEE 802.1Q (VLAN), 802.1p (QoS), 802.3x (Flow Control), 802.1Qbb (PFC), 802.1Qaz (ETS)

- IEEE 802.3bj, 802.3cd, 802.3ck for 100G/400G Ethernet

- RFC 3168 (ECN), RFC 2474 (DiffServ), RFC 3246 (EF PHB)

- RoHS, WEEE, REACH environmental directives

- Safety: UL 60950-1, IEC 60950-1, EN 60950-1

- EMC: FCC Part 15 Class A, EN 55032 Class A, EN 55024

TECHNICAL SPECIFICATIONS

Parameter	**Specification**
Form Factor	1RU Fixed Configuration / Modular Chassis Option
Switching Capacity	3.2 Tbps to 12.8 Tbps (depending on

	SKU)
Packet Buffer Memory	64 MB to 128 MB Fully Shared On-Chip Pool
Microburst Absorption Duration	> 10 ms at 100% Line Rate per Port
Forwarding Rate	Up to 9.5 Bpps (Billion Packets Per Second)
Port Configurations	48x25G + 8x100G / 32x100G + 4x400G
Power Supply	Dual Hot-Swappable Redundant AC/DC (1+1)
Cooling	Front-to-Back or Back-to-Front Airflow Fan Trays
QoS Queues	8 Queues per Port, Strict Priority + DWRR
Congestion Management	PFC, ECN, Dynamic Buffer Thresholding, WRED
Management	CLI, SNMPv3, RESTCONF, gRPC, Telemetry Streaming
Operating Temperature	0°C to 45°C (Commercial), -5°C to 55°C (Extended)
MTBF	> 250,000 Hours
Dimensions (HxWxD)	44 x 440 x 450 mm (1RU)
Weight	8.5 kg (fully loaded)

ORDERING SKU INFORMATION

Base System:

- AGG-DBM-48Y-8C: 48 x 25G SFP28 + 8 x 100G QSFP28 Aggregation Switch, Dual AC PSU, 3+1 Fan Tray

- AGG-DBM-32C-4D: 32 x 100G QSFP28 + 4 x 400G QSFP-DD Aggregation Switch, Dual AC PSU, 4+1 Fan Tray

Optional Accessories:

- PSU-AC-1600W: 1600W Hot-Swappable AC Power Supply Unit

- FAN-TRAY-3RU: Spare Fan Tray Module for 1RU Chassis

- RAIL-KIT-1RU: Universal 4-Post Rack Mount Rail Kit

